REMARKS

I. Introduction

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claims 5-17 Under 35 U.S.C. § 103

Claims 5-8, 13 and 15-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Keys (US 2004/0235280) in view of Li (USP No. 7,094,671); claims 9 and 12 as being unpatentable over Yu (USP No. 6,521,502); claim 10 as being unpatentable over Yu in view of Keys; claim 11 as being unpatentable over Yu in view of Li; and claim 14 as being unpatentable over Keys in view of Li and further in view of Yu. Applicants respectfully traverse these rejections of the pending claims for at least the following reasons.

With regard to the present invention, amended claims 5, 9 and 13 disclose, in-part, a method for manufacturing a semiconductor device that comprises the successive steps of: (a) forming an amorphous layer; (b) heat treating the amorphous layer without implanting ions into the amorphous layer, thereby reducing the depth of the amorphous layer and restoring a crystal structure of the amorphous layer in a region from a first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; and (c) after the heat treating step, introducing an ion impurity into the heat-treated amorphous layer.

The amorphous layer shrinks to a shallower depth (second depth) in the substrate during the reducing depth step, with defects that are generated in the forming the amorphous layer step remaining at the deeper depth (first depth) in the substrate. Using these steps, a source/drain region is formed by implanting an impurity into the depth-reduced amorphous layer, while

avoiding effects from the defects existing in the deeper depth. As a result, it is possible to obtain a transistor in which a leakage current caused by defects is suppressed.

With regard to the rejection of claims 5 and 13, it is admitted in the Office Action that Keys discloses the step of implanting ions into the amorphous layer. Li is used to remedy this deficiency. However, Li discloses implanting Ge ions into the workpiece 202 to form an amorphous layer 230 containing Ge and a crystalline layer 236 containing Ge. At the boundary of these layers, a damage region 234 occurs. Then, the entire amorphous layer 230 is crystallized to a crystalline layer 238 by heat treatment, followed by ion implantation into the crystalline layer. Accordingly, Li fails to disclose a step of a step of forming an amorphous layer in a region from a first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth, or, after the heat treating step, introducing an ion impurity into the heat-treated amorphous layer. As such, the combination of Li and Keys fails to disclose each and every limitation of claims 5 and 13 of the present disclosure.

Regarding the rejection of claim 9 over Yu, it is alleged that Yu discloses reducing the depth of an amorphous layer from a first depth to a second depth by a heat treatment and forming impurity layers 20 and 22 by introducing ions into the heat treated amorphous layers. Further, it is alleged that the impurity layers 50 and 52 are formed in the amorphous layers whose depth is reduced by a heat treatment. However, in Yu, amorphous layers 25 are formed by implanting Si or Ge. Next, ion implantation is performed without changing the depth of the amorophous layers. This is then followed by ion implantation and then heat treatment, which transforms the structure of the regions from amorphous to a single crystalline state. Thus, the Office Action misinterprets Yu and as such, Yu fails to disclose the step of reducing the depth of the amorphous layer and restoring a crystal structure of the amorphous layer in a region from a first

depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth.

As is well known in patent law, in order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. As is clearly shown above, Keys, Li and Yu do not disclose a method for manufacturing a semiconductor device that comprises the successive steps of: (a) forming an amorphous layer; (b) heat treating the amorphous layer without implanting ions into the amorphous layer, thereby reducing the depth of the amorphous layer and restoring a crystal structure of the amorphous layer in a region from a first depth to a second depth that is shallower than the first depth so that the amorphous layer shrinks to the second depth; and (c) after the heat treating step, introducing an ion impurity into the heat-treated amorphous layer. Therefore, Applicants submit that Keys, Li and Yu do not render claims 5, 9 and 13 of the present invention obvious and accordingly, Applicants respectfully request that the § 103(a) rejection of claims 5, 9 and 13 be withdrawn.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 5, 9 and 13 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having responded to all open issues set forth in the Office Action, it is respectfully submitted that all claims are in condition for allowance.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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